

**WHAT IS CLAIMED IS:**

1. A data transmission system for transmitting a payload constituted from a number of concentrated signals, the system comprising:

a demultiplexer having an input for coupling to the payload and having plurality of outputs;

a multiplexer have a plurality of inputs;

a plurality of pointer processors, each having an input coupled to a respective output of the demultiplexer and having an output coupled to a respective input of the multiplexer, wherein each of the pointer processors comprises:

(a) a bidirectional terminal coupled to a common node, and

(b) circuitry coupled to the processor input, processor output and bidirectional terminal, the circuitry for:

(i) causing a logic level to be asserted at the common node in response to an error signal at the processor input, and

(ii) causing an alarm signal to appear at the processor output in response to the application of a logic level signal at the processor bidirectional terminal.

2. A data transmission system as defined in Claim 1, wherein the bidirectional terminal of each of the plurality of processors is coupled to the common node and the common node is coupled through a resistance to a voltage,  $V^+$ , so that in the absence of an alarm signal at all the processor inputs, the voltages at the bidirectional terminals of the processors approaches  $V^+$ .

3. A data transmission system as defined in Claim 2, wherein as a result of an error signal at the input of any processor, the voltages at the bidirectional terminals of all the processors approach a reference voltage.



- 8 (i) causing a predetermined logic level to be asserted at the common node in response to  
9 an error signal at the processor input, and  
10 (ii) causing an alarm signal to appear at the processor output in response to the  
11 application of the predetermined logic level at the processor bidirectional terminal.

1 8. A pointer processor as defined in Claim 7, wherein the alarm means includes an  
2 error detector for detecting an error in a signal that is included as a component of a concatenated  
3 payload.

1 9. A pointer processor as defined in Claim 8, wherein the error detector detects the  
2 presence of an STS-Nc signal.

1 10. A pointer processor as defined in Claim 8, wherein the error detector detects one  
2 or more of the following errors in a SONET-compliant system: LOS, LOF, AIS\_L and LOP.

1 11. A pointer processor as defined in Claim 7, wherein the alarm means comprises:  
2 an error detector;  
3 a wired-OR logic element coupled between the error detector and the bidirectional terminal; and  
4 a combinational logic element having inputs respectively coupled to the error detector and the  
5 wired-OR logic element and an output coupled to the output of the processor.

1 12. A pointer processor as defined in Claim 11, wherein the error detector detects the  
2 presence of an STS-Nc signal.

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